

Glorifying the If-Statement

PHMon: A Programmable Hardware Monitor and Its Security Use Cases

Leila Delshadtehrani, Sadullah Canakci, Boyou Zhou, Schuyler Eldridge, Ajay Joshi, and
Manuel Egele

Nathan S. Rutherford

Email: nathan.rutherford.2019@live.rhul.ac.uk

Twitter: @rutherfordns

Website: nsrutherford.com

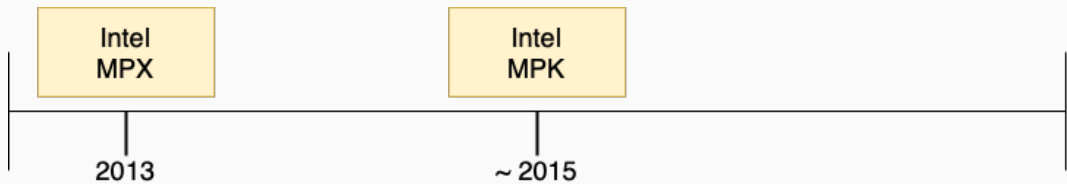
18th November 2020

Royal Holloway, University of London

A horizontal timeline with a central line. A vertical tick mark is on the left, and another is on the right. A yellow box labeled 'Intel MPX' is positioned above the line, starting from the left tick mark. A vertical line connects the bottom of the box to the year '2013' below the line.

Intel
MPX

2013



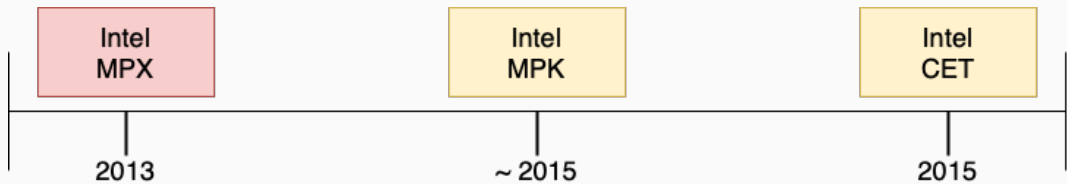
Intel
MPX

A horizontal timeline with two vertical tick marks. A red box labeled 'Intel MPX' is positioned above the first tick mark, and a yellow box labeled 'Intel MPK' is positioned above the second tick mark.

2013

Intel
MPK

~ 2015



Intel
MPX

2013

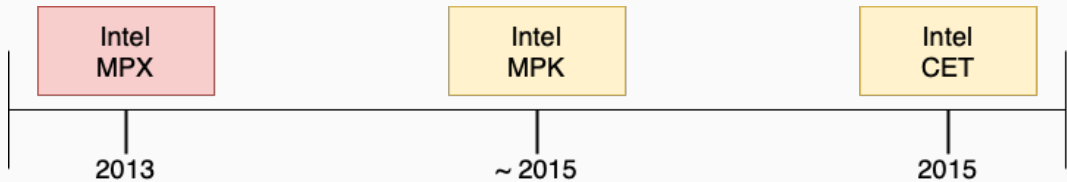
Intel
MPK

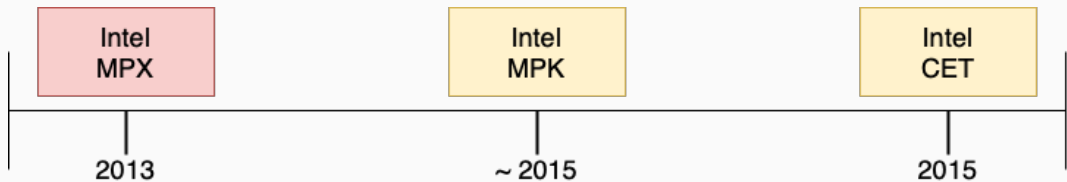
~ 2015

Intel
CET

2015







PHMon

Use-cases

Hardware Accelerated Fuzzing

Evaluation

Conclusion

PHMon

Programmable Hardware Monitor

Programmable Hardware Monitor

Event-Action Monitoring Model

Programmable Hardware Monitor

Event-Action Monitoring Model

Three Stage Pipeline:

Programmable Hardware Monitor

Event-Action Monitoring Model

Three Stage Pipeline:

- Collect

Programmable Hardware Monitor

Event-Action Monitoring Model

Three Stage Pipeline:

- Collect
- Examine

Programmable Hardware Monitor

Event-Action Monitoring Model

Three Stage Pipeline:

- Collect
- Examine
- Action

Trace Unit (TU)

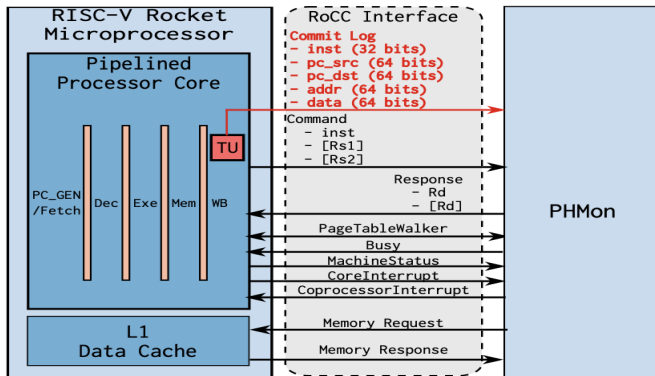


Figure 2: The RoCC interface extended with *commit log* execution trace.

Match and Action Units (MU & AU)

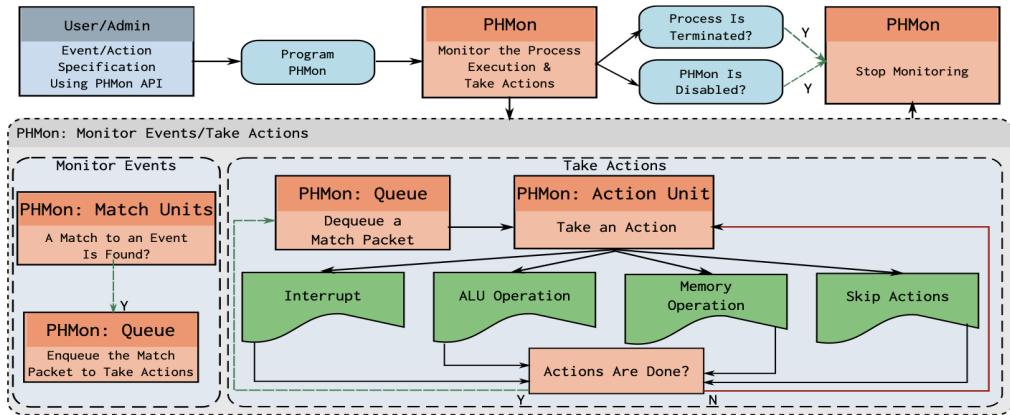


Figure 1: An overview of the *event-action* model provided in PHMon.

Use-cases

Shadow Stack Protection

Shadow Stack Protection

Hardware Accelerated Fuzzing

Potential Use-cases

Shadow Stack Protection

Hardware Accelerated Fuzzing

Prevention of Information Leakage

Potential Use-cases

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Hardware Accelerated Fuzzing

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Watchpoints and Accelerated Debugger

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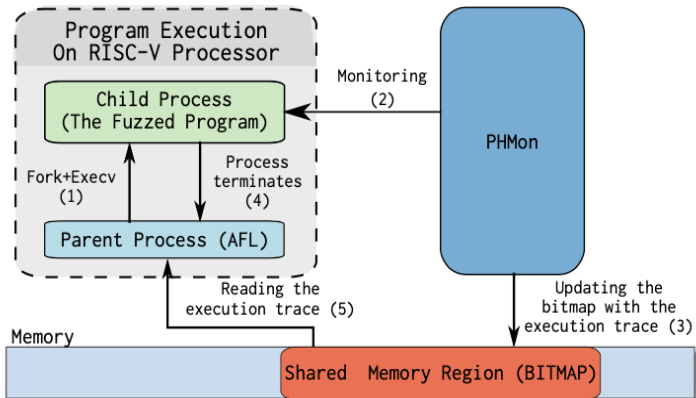


Figure 4: Integration of PHMon with AFL.

Evaluation

Evaluate performance of the aforementioned four use-cases

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RISC-V Rocket Chip with PHMon as RoCC

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PHMon implemented on Xilinx FPGA

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Linux v4.15 Target

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PHMon implemented on Xilinx FPGA

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Disclaimer:

No L2 Cache on set-up that may have impacted performance

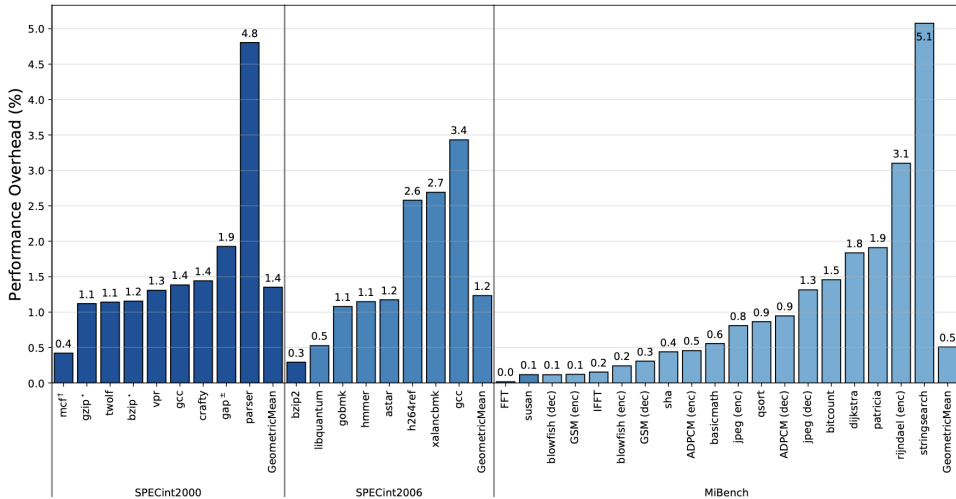


Figure 5: The performance overhead of PHMon as a shadow stack.

[†] We were not able to run mcf benchmark with reference input on our evaluation board; as a result, we used the test input for this benchmark.

* Due to the memory limitations of our evaluation board, we had to reduce the buffer size of the reference input to 3 MB for gzip and bzip2 benchmarks.

[‡] We had to use -O0 and an input buffer size of 96 MB to successfully run gap benchmark.

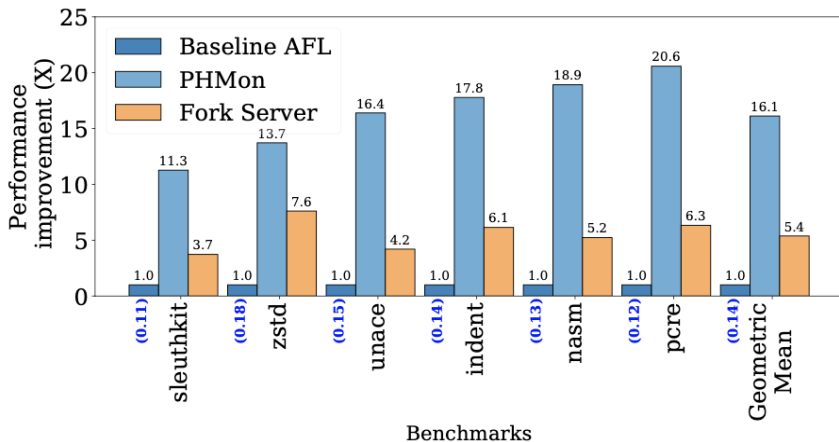


Figure 6: Performance improvement of PHMon over the baseline AFL compared to fork server AFL. The numbers below the “Baseline AFL” bars show the number of executions per second for the baseline AFL.

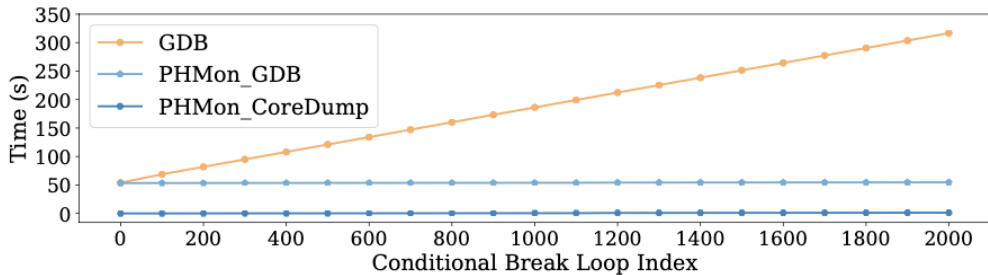


Figure 7: The performance overhead of PHMon compared to GDB for a loop conditional breakpoint.

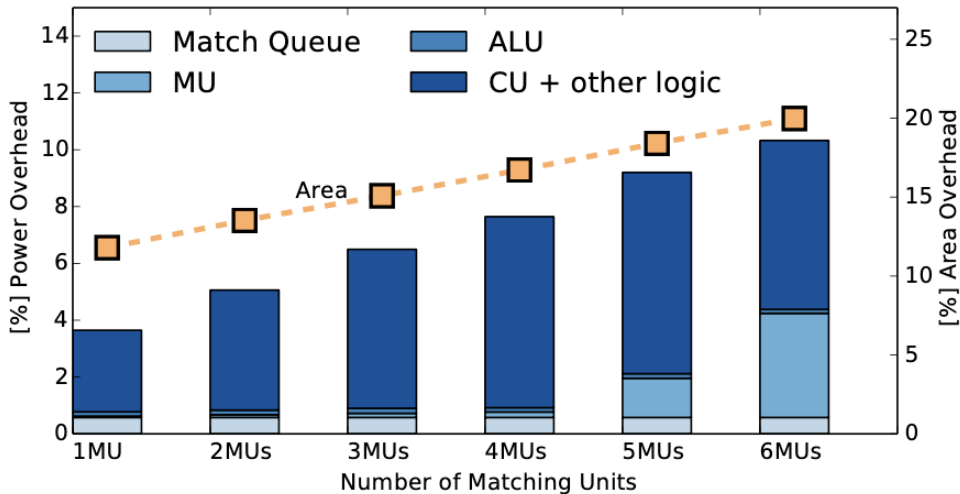


Figure 8: The power and area overheads of PHMon components compared to the baseline Rocket processor.

Conclusion

Well motivated and reasonable approach

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Recontextualising of Match-Action Pipeline for security monitoring in an OS

Well motivated and reasonable approach

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Fidelity and impact for research I would expect for USENIX

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Simplistic Threat Model

Popular hardware approaches only enforce a static security policy

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PHMon is a flexible hardware monitor leveraging an Event-Action Pipeline

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Evaluation shows .9% overhead for shadow-stack protection

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Improves performance of AFL by up to 16x, finding more bugs

Questions

1. Are there any caching opportunities for PHMon that could improve performance?
2. Does PHMon deal with branch prediction in monitoring?
3. Can monitoring rules be updated in real-time, or does it require PHMon to be offline?