Leveraging Hardware Capabilities for Building Dependable Many-Core Operating Systems

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Objectives

- Distributed kernel design to support fault tolerance
- Treat specialised processors as first-class citizens in the operating system
- Provide cross-domain process communication (XPC) and enforce core isolation and security policies using hardware capabilities
- Flexible abstraction model to support hardware accelerators

Introduction

Post-Moore's Law computer architectures are moving towards:

- Specialised Processor Technology (SPT) [7]
- General Processor Technology (GPT) that increase the number of cores
- Operating System (OS) designs that support heterogeneity [6]

Multikernel architectures like Barrelfish [2] emerged to support growing core count:

- Treats multi-core systems as a distributed system running a separate kernel per core
- Not suitable for specialised devices that cannot run an OS Kernel e.g. GPUs [5]

Most research centred around performance and scalability

- Little focus on dependability

Background

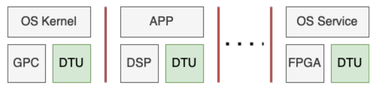


Figure 1: Architecture diagram of the M^3 system adopted from [1]

M^3 [1]

- Network-on-a-chip level isolation
- Common hardware interface via Data Transfer Unit (DTU)
- Extended to support distributed capabilities model [3]

CHERI [8]

- Capabilities part of the chips Instruction-Set-Architecture (ISA)
- Security policy enforced by the hardware
- Built-in spatial memory safety
- Temporal safety possible

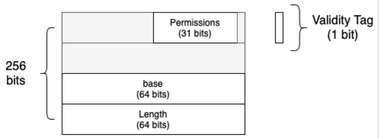


Figure 2: Original CHERI capability visualisation from [8]

Early System Design

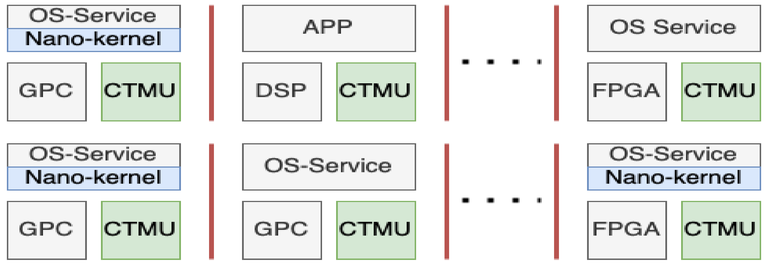


Figure 3: Early system diagram with a distributed nano-kernel for OS management and a Capability Transfer and Management Unit (CTMU) for supporting communication between heterogeneous cores and enforcing fine-grained security policy

Overview

Distributed kernel architecture supported by a CHERI-aware hardware chip, treats kernel management as a multi-core consensus problem

Capability Transfer and Management Unit (CTMU)

- Manages enforcement of security policy
- End-point for cross-core communications

Nano-kernel

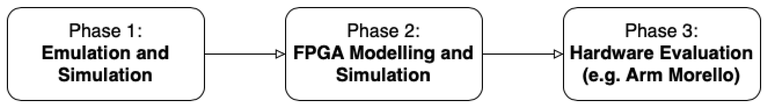
- Optional component as not all cores may support it
- Resource management function
- Replicated across all nano-kernel instances via consensus
- Quick recovery time on failure, or in periods of high utilization in a region

Flexible Abstraction Model

- Null-kernel composition [4]
- Treat hardware accelerators as first-class citizens

Evaluation Plan

Two-phase evaluation, with an optional third phase depending on hardware availability



Key Performance Metrics:

- Fault Tolerance & Recoverability
- Latency

Research Opportunities

- 5G Infrastructure
- Native interfaces for cryptography accelerators
- Media encoding
- Datacenters

Conclusions

- Most many-core designs treat the OS as a distributed system, however few focus on dependability
- We propose a many-core OS design leveraging hardware capabilities to distribute the kernel across cores, allowing higher levels of fault-tolerance and enabling rapid recoverability

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